## Chapter 1. EMMC Controller

### 1.1 Overview

DWC\_mshc provides a flexible bus interface that enables you to integrate DWC\_mshc into embedded applications for system-on-a-chip (SoC) designs. DWC\_mshc has an AXI and AHB master interface that supports 32-bit and 64-bit address and data bus. Besides supporting non-DMA mode, DWC\_mshc supports various DMA options such as SDMA, ADMA2, and ADMA3 as specified in the SD Host Controller Standard.

### 1.2 Block Diagram



Fig. 1.1 emmc controller module block diagram

### 1.3 Features

■ Supports eMMC protocols including eMMC 5.1  
■ Supports the following data transfer types for eMMC modes

❑ CPU

❑ SDMA

❑ ADMA2

❑ ADMA3  
■ Supports independent Core, Slave Interface and Master Interface clocks  
■ Supports gating of core base clock if Host Controller is inactive  
■ Support context aware functional clock gates  
■ Applications can gate the slave interface clock if Host Controller is inactive  
■ Data Buffering  
 ❑ Configurable buffer depth. Configurable in coreConsultant/coreAssembler

❑ Automatic packing/unpacking of data to fit buffer width

■ Interrupt Outputs

❑ Combined and separate interrupt outputs

❑ Supports interrupt enabling and masking  
■ Supports Slave-Only mode as a configuration option for better area and power efficiency  
■ Supports tuning  
■ eMMC Tuning using CMD21 (eMMC)  
■ Mode 1 Re-Tuning – Host driver maintains the re-tune timer  
■ Fully Software driven Tuning/Re-tuning operations